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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,784	07/28/2003	Takeshi Ohi	402720	5342

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,784	OHI ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed on 08-03-04 has been received and entered in the case. New ground of rejections necessitated by the amendment is set forth below.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitation "controllable variable value detection means", "abnormal detection means " in claims 1-7 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 3, the recitation "during a transition time....,a predetermined value" on lines 3-8 is indefinite because it is not clear what "when said control means **receives** a turn -on instruction and **ends** before a control voltage that appears at the control terminal of the power semiconductor device reaches..." is meant by. The Applicant is requested to explain clearly what is the "a transition period" and when it start, when it ends and what is a "predetermined voltage value".

Claim 4 is indefinite because it is not clear what is the "a transition time period"; when it begins; when it ends; " what is the "**expiration** (?) of a time interval after said has received a turn-on instruction and ends before a control voltage that appears at the control terminal of the power semiconductor device reaches". As understood by the examiner, if the turn-on signal is a pulse having an on-time T and no abnormality occurs during time T, the power semiconductor device is turned on during interval of time T. If during time T, the "controllable variable value detection means" detects an abnormality (a "predetermined voltage value") at the gate of the power semiconductor device, the power semiconductor device is turned off. The Applicant is requested to clarify claim 4 and to show in what drawing, the circuit of claims 4 reads on and to explain clearly what is the "a transition period" and when it starts, when it ends and what is a "predetermined voltage value".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5 and 7 are rejected under 35 U.S.C 102(e) as being anticipated by Fukuda et al. (US Pat. 6,717,785).

Regarding claim 1, figure 13 of Fukuda shows a drive circuit for driving a power semiconductor device, said circuit comprising:

control means (GATE DRIVING CIRCUIT) for controlling switching of the power semiconductor device (51) according to a turn-on instruction or turn-off instruction sent to the power semiconductor device from outside said drive circuit;

" controllable variable value detection means" (R4, R3) for detecting value of an electrical variable controlled by said control means and that is applied to a control terminal (gate) of the power semiconductor device (51) during a time period when said control means receives a turn-on instruction; and

"abnormality detection means" (Tr1, Tr2, R5) for monitoring the value detected by said controllable variable value detection means to detect occurrence of an abnormality (over-current) in the power semiconductor device. During normal operation, the voltage at the gate of transistor (51) is smaller that the threshold (Vbor). After the turn-on instruction, transistor (51) is turned on, transistor (Tr1) is turned off and transistor (Tr2) is turned on. The node between (R1) and (R2) is shorted to ground and transistor (Tr3) is turned off. When over-current (abnormality) occurs, the voltage at the gate of transistor (51) rises beyond the threshold voltage (Vbor). As a result, transistor (Tr1) is turned on, transistor (Tr2) is turned off, the voltage applied to the gate of transistor (Tr3) rises, transistor (Tr3) is turned on and transistor (51) is shut off.

Regarding claims 2 and 3, the " controllable variable value detection means" detects the voltage (charge) applied to the gate (control terminal) of the power semiconductor device (51) when the transistor (51) is turned on. When the voltage at the gate of transistor (51) rise because of an abnormality (over-current), transistor (51) is turned off.

Regarding claims 4 and 5, when the control means sends a signal to turn switch (51) on in a period of time, the voltage at the gate of transistor (51) starts to rise to turn transistor (51) on. When the over-current occurs, the voltage at the gate of transistor (51) reaches a predetermined threshold, the "controllable variable value detection means" (R3, R4) detects that voltage and the "abnormality detection means" (Tr1, Tr2, R5) sends a signal to transistor (Tr3) to turn off transistor (51).

Regarding claim 7, figure 13 of Fukuda shows a drive circuit for driving a power semiconductor device (51), said circuit comprising:

control means (GATE DRIVE CIRCUIT);

controllable variable value detection means (R3, R4);

abnormality detection means (Tr1, Tr2, R5). During normal operation, the voltage at the gate of transistor (51) is smaller that the threshold (Vbor). After the turn-on instruction, transistor (51) is turned on, transistor (Tr1) is turned off and transistor (Tr2) is turned on. The node between (R1) and (R2) is shorted to ground and transistor (Tr3) is turned off. When over-current (abnormality) occurs, the voltage at the gate of transistor (51) rises beyond the threshold voltage (Vbor). As a result, transistor (Tr1) is turned on, transistor (Tr2) is turned off, the voltage applied to the gate of transistor (Tr3) rises, transistor (Tr3) is turned on and transistor (51) is shut off.

Response to Arguments

In the Remarks, page 4, lines 27-29, the Applicant explains that "When that value is **reached**, or **not reached** if **total charge** flowing into the gate is monitored, during the time period, **then it is apparent that an abnormality has occurred** and appropriate action is to be taken" is not clear. It is not clear why the "abnormality" occurs in **both conditions**: when the gate voltage **reaches** the threshold voltage and when the gate voltage **does not reach** the threshold voltage. The Applicant is requested explain what is "total **charge** flowing into the gate" and to clarify claims 3 and 4 because they are ambiguous.

Allowable Subject Matter

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 6 is objected to because the prior art of record fails to teach or fairly suggest a drive circuit having a control means causes said power semiconductor device to make a transition to an off state at a lower speed than that at which said control means causes said power semiconductor device to make a transition to an off state according to a turn-off instruction.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
10-12-04

TUAN T. LAM
PRIMARY EXAMINER